

gate, the wide recess and the gate recess, and another mask to form the source and drain contacts.

**[0010]** First, we have discovered that there is a problems caused by over-etching the portions of Ultra-Thin (UT) Silicon-On-Insulator (SOI) in CMOS FET devices in close proximity to the spacers during the spacer etching process. Accordingly there is a need to overcome that problem.

**[0011]** In addition, we have discovered that it is difficult to control Raised Source and Drain (RSD) epitaxy, especially on a doped surface. In accordance with this invention, a Si/SiGe/SOI structure can be employed to manufacture UT-SOI CMOS devices.

#### SUMMARY OF INVENTION

**[0012]** An object of this invention is to provide a manufacturable method and a device structure that overcomes the problems described above.

**[0013]** This invention teaches a controlled manufacturable method of selectively recessing the channel region is such a way that the extension regions remain thick so that no raised source drain process is needed.

**[0014]** In accordance with this invention, a method is provided for manufacturing Ultra-Thin SOI CMOS FET Devices with Raised Sources and Drains (RSD) Using Recessed Channels and Structures Manufactured Thereby.

**[0015]** The method starts with a relatively thick modified SOI structure comprising Silicon/Silicon Germanium/Silicon on an insulator (Si/SiGe/Si-on-insulator), which is thick enough for the spacer etch.

**[0016]** A SiGe layer and a top Si layer are used as etch stoppers to obtain good control of the channel thickness, which is important for the control of  $V_t$ , mobility, and the Short Channel Effect (SCE) of UT-SOI devices.

**[0017]** In accordance with this invention a method is provided for forming an RSD FET device with a recessed channel, a raised silicon S/D, and a gate electrode structure on an SOI structure as follows. Form a SiGe layer over the silicon layer and a RSD layer over the SiGe. Etch through the RSD layer and the SiGe to form a gate electrode space reaching down the silicon layer. Form a pair of RSD regions separated by the gate electrode space. Line the walls of the gate electrode space with an internal etch stop layer and an inner sidewall spacers. Form a gate electrode inside the inner sidewall spacers on the silicon layer. Form external sidewall spacers adjacent to the gate electrode between the RSD regions next to the inner sidewall spacers, and dope the RSD regions, whereby a recessed channel is formed in the SOI silicon layer between the raised source/drain regions above the SiGe layer. Preferably, an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space. Preferably, the steps of forming the gate electrode space include the following steps. Form a dummy gate over the source/drain layer; form a conformal outside spacer layer over the dummy gate; form an exterior masking layer over the outside spacer layer, etching back the exterior masking layer to expose the dummy gate, and remove the dummy gate to form the gate electrode space. Preferably, the exterior masking layer is composed of silicon dioxide that covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof.

Preferably, the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer. Preferably, the insulator forming the substrate comprises silicon oxide. Preferably, an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space, and the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof and after recessing the outside spacer layer down to the etch stop layer. Preferably, an etch stop layer is formed on the surface of the raised source drain layer before forming the gate electrode space; the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and planarization thereof. After recessing the outside spacer layer down to the etch stop layer, perform a raised source extension region and a raised drain extension region implant and then form an exterior spacer aside from the gate electrode.

**[0018]** In accordance with another aspect of this invention, a method is provided for forming an FET device with a raised silicon source/drain and a gate electrode structure on an SOI structure comprising an SOI silicon layer formed on a substrate wherein the substrate comprises an insulator, whereby a recessed channel is formed in the SOI silicon layer between the raised source/drain regions above the SiGe layer as follows. Form a SiGe layer over the silicon layer. Form a raised source/drain layer over the SiGe layer. Form an etch stop layer over the raised source/drain layer. Form a dummy gate over the source/drain layer. Form a conformal outside spacer layer over the dummy gate. Form an exterior masking layer over the outside spacer layer. Etch back the exterior masking layer to expose the dummy gate. Remove the dummy gate to form the gate electrode space etching through the raised source/drain layer and the SiGe layer to form a gate electrode space with walls reaching down through the raised source/drain layer and the SiGe layer to the surface of the silicon layer thereby forming a pair of raised source/drain regions separated by the gate electrode space in the source/drain layer. Line the walls of the gate electrode space with an internal etch stop layer and an inner sidewall spacers. Form a gate electrode inside the inner sidewall spacers on a cleaned surface of the silicon layer. Form external sidewall spacers adjacent to the inner sidewall spacers. Dope the source/drain regions.

**[0019]** Preferably, an exterior masking layer is formed composed of silicon dioxide which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and performing planarization of the gate electrode. Then strip the exterior masking layer. Form the exterior masking layer of silicon germanium (SiGe) which covers the outside spacer layer until after filling the gate electrode space with the gate electrode and after planarization of the gate electrode; and then recess the outside spacer layer down to the etch stop layer adjacent to the gate electrode. Preferably, the insulator forming the substrate comprises silicon oxide.

**[0020]** Preferably, the exterior masking layer is composed of silicon germanium (SiGe) which covers the outside